REMARKS

Claims 1, 11, 20, 29 and 36 have been amended for clarification. Claims 1-36 are currently pending and under consideration. Reconsideration is respectfully requested.

I. REJECTION OF CLAIMS 1-3, 6-22 AND 25-36 UNDER 35 U.S.C. 103(A) AS BEING UNPATENTABLE OVER TAGUCHI (U.S. PATENT NO. 5,915,025)(previously cited) IN VIEW OF CURRAN (U.S. PATENT NO. 4,525,599)(previously cited):

Claim 1 has been amended to recite "an internal circuit comprising: a CPU executing programs, at least one internal device having a predetermined function, and **a bus line extending internally of the internal circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the internal circuit and an address bus and a data bus transferring an address and data, respectively**, wherein said internal circuit includes at least one internal memory as an internal device".

As previously mentioned, Taguchi discloses a data processing apparatus with software protection functions capable of changing encryption-decryption algorithms. The data processing apparatus comprises a data processing means, distributed software decryption means, encryption means, decryption means, and key supply means. The encryption means and decryption means are capable of changing encryption or decryption algorithms. The data processing apparatus also includes algorithm supply means for supplying encryption-decryption algorithm programs. An encryption method selection means selects keys and algorithms to be supplied to the encryption and decryption means (see column 21, lines 5-56; and FIGS. 23 and 31). Taguchi also discloses a system bus, a storage means, an I/O interface, a peripheral bus, an Ethernet controller, a CD-ROM drive and a hard disk drive. When a software supplier supplies a user with data encrypted by a predetermined encryption method over the network or by means of a CD-ROM, the user sends the encrypted data and an encryption key to the distributed software decryption means through the I/O interface. The distributed software decryption means decrypts the encryption key and then target data by utilizing the decryption encryption key. The decrypted data is forwarded directly to the encryption means and the encryption means encrypts the received data using the encryption algorithm and encryption key selected by the encryption method selection means and places the encrypted data in the storage means. The encrypted data remains encrypted in the storage means and is decrypted by the decryption means and sent to the data processing for data execution (see column 21, lines 58-61).

At page 3 of the Office Action, the Examiner asserts that the system bus 40 shown in FIG. 3 of Taguchi is both internal and external to the secure protective enclosure 150. However, the Applicants respectfully disagree. As shown in FIG. 3 the system bus 40 is external to the enclosure 150. That is, it is not internally positioned within the enclosure 150 itself (see column 9, lines 61-63, for example).

At page 4 of the Office Action, the Examiner asserts that the protective enclosure 150 in FIG. 31 is comparable to the Applicants' "internal circuit" and that the arrows between the data processing means 151 and the decryption means 154 and encryption means 153 corresponds to the Applicants "bus line 110" shown in FIG. 1 of the present invention. The Examiner also asserts that "bus line 160" of Taguchi is comparable to the Applicants "bus line 110a" and extends externally and transfers data between elements 152, 153, 154 and 160.

Further, at the bottom of page 4, the Examiner states that the Applicants "bus line" comprises an externally extending portion extending externally of said **external** circuit. This assertion is incorrect. The Applicants respectfully submit that the present invention recites "a bus line...comprising an externally extending portion extending externally of said **internal** circuit," as recited in claim 1, for example.

The Applicants respectfully submit that the arrows between the data processing means 151 and the encryption means 153 and decryption means 154 in FIG. 31 of Taguchi are not comparable to the Applicants' "bus line" as recited in amended claim 1, for example. That is, these arrows do not constitute "a bus line", and therefore these arrows do not transfer both an address and data. Instead, these arrows merely transfer data from the data processing means 151. Therefore, Taguchi fails to disclose "a bus line extending internally of the internal circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the internal circuit and an address bus and a data bus transferring an address and data, respectively," as recited in amended claim 1, for example.

As mentioned above, the Applicants' "bus line" as recited in claim 1, for example, is capable of transferring both address and data. Therefore, the teachings of Taguchi are fundamentally different from that of the present invention.

At page 6 of the Office Action, the Examiner admits that Taguchi fails to disclose "ciphering an address" as disclosed in claim 1 of the present invention, for example. The Examiner also admits that Taguchi fails to disclose the processing means being provided with cache memory. However, the Examiner's asserts that Curran teaches software can be protected from illegal copying by encrypting the addresses of the data being accessed in order

to provide a non-sequential ordering of the data in memory as well as encrypting the data stored therein. Therefore, the Examiner asserts that it would be obvious to one skilled in the art to modify Taguchi to include the features of Curran. The Applicants respectfully traverse the Examiner's assertion.

As previously mentioned, Curran merely discloses an apparatus to prohibit the unauthorized copying of computer software information such as electronic video games, by encrypting the program information stored in the memory and by implementing encryption /decryption circuitry interposed between the memory and the central processor in a fashion such that any attempt to dump the decrypted program through use of a microprocessor emulator is detected and stopped (see column 1, lines 50-59). That is, upon detection of the invalid program event or "trap condition" the protection circuit switches to its second operating mode thereby to prevent copying of the decrypted program information (see Abstract). The Applicants respectfully submit that there is no motivation to combine Taguchi and Curran. The teachings of Curran are unrelated to those of Taguchi and the present invention. That is, Curran is related to preventing copying a video game, for example. Therefore, Curran fails to disclose "an external circuit" as recited in claim 1, for example. Curran also fails to disclose "wherein said internal circuit includes a ciphering section interposed at an entrance to an external side of said internal circuit, and ciphering the address and the data on the bus line by ciphering patterns according to a plurality of regions divided from an address space allotted to entirety of said at least one external device, to thereby prevent illicit access to the internal memory via the external memory," as recited in claim 1.

Therefore, the Applicants respectfully submit that there is no motivation to combine Taguchi and Curran. Thus, the Examiner's combining of Taguchi and Curran fails to establish a prima facie case of obviousness over the present invention.

Independent claims 11, 20, 29 and 36 recite similar features as those of amended claim 1. Thus, although the above comments are specifically directed to claim 1, it is respectfully submitted that the comments would be helpful in understanding differences of various other rejected claims over the cited references. Therefore, it is respectfully submitted that the rejection is overcome.

II. REJECTION OF CLAIMS 4 AND 23 UNDER 35 U.S.C. 103(a) AS BEING UNPATENTABLE OVER TAGUCHI IN VIEW OF CURRAN AND FURTHER IN VIEW OF IBM (IBM TECHNICAL DISCLOSURE BULLETIN-19800601):

The comments in section II above may be applied here, where applicable.

III. REJECTION OF CLAIMS 5 AND 24 UNDER 35 U.S.C. 103(a) AS BEING UNPATENTABLE OVER TAGUCHI IN VIEW OF CURRAN AND FURTHER IN VIEW OF MILHAUPT (U.S. PATENT No. 5,706,445)(previously cited):

The comments in section II above may be applied here, where applicable.

IV. CONCLUSION:

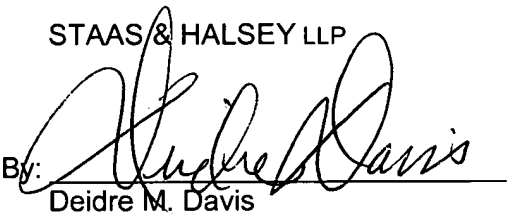
In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 7/26/2006

By: 

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